Gate Bias and Geometry Dependence of Total-Ionizing-Dose Effects in InGaAs Quantum-Well MOSFETs

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35-word abstract

The effects of total-ionizing-dose irradiation are investigated in InGaAs quantum-well MOSFETs. Irradiation and stress effects are additive or compensatory to each other, depending on gate bias. The degradation increases with the channel length.

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INTRODUCTION

Many III-V materials, due to their high electron mobilities and high injection velocities, are promising channel candidates for future logic applications [1]. In particular, the InGaAs MOSFET is considered the leading candidate for the n-channel device for sub-10 nm CMOS technology nodes [2]. To operate in space environments, InGaAs MOSFETs must be able to withstand ionizing radiation.

In this paper, we investigate total-ionizing-dose (TID) effects in InGaAs quantum-well MOSFETs with a thin (2.5 nm) HfO_2 gate dielectric. Preliminary TID effects have been reported in InGaAs planar MOSFETs and gate-all-around MOSFETs [3], [4] as well as AlGaN/GaN MOS HEMTs [5], but all of these devices use a thick Al_2O_3 oxide with an effective oxide thickness (EOT) of approximately 5 nm. High densities of defect states at the high κ/semiconductor interface and in the high κ layer can cause positive bias temperature instability, especially in InGaAs MOSFETs [6]. Hence, it is important to investigate TID effects in these structures and separate the TID response from effects produced by bias alone. In this work, we evaluate the gate bias and geometry dependence of TID and bias-stress effects for InGaAs quantum-well MOSFETs with thin (2.5 nm) HfO_2 gate dielectrics (EOT of about 0.5 nm). This is a much more relevant gate dielectric for future CMOS applications. We find that irradiation and stress effects on threshold voltage are additive or partially offsetting, depending on gate bias. The magnitude of the changes in threshold voltage and degradation in transconductance increases with the channel length.

EXPERIMENTAL DETAILS

The devices considered here are self-aligned InGaAs quantum-well MOSFETs. The detailed fabrication process is described in [7]. Fig. 1(a) shows a schematic cross section of the device (not drawn to scale). A 0.4 μm thick $In_{0.52}Al_{0.48}As$ buffer layer is grown on a 600 μm thick semi-insulating InP substrate. A 5 nm thick $In_{0.7}Ga_{0.3}As$ channel is grown on top of the buffer layer. A silicon delta doping layer (*n*-type) in the buffer just below the channel is used to enhance the channel electron density. 2.5 nm of HfO_2 is deposited by atomic layer deposition directly on top of the channel. Fig. 1(b) shows the measured capacitance from 300 kHz to 5 MHz. The capacitance equivalent thickness (CET) in these devices is approximately 1.7 nm. The vertical energy band alignment through the gate is described in [8].

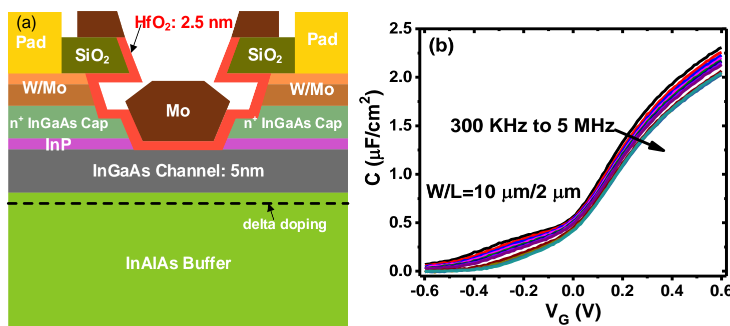

Fig. 1 (a) Schematic cross section of the device under test (not drawn to scale); (b) measured capacitance as a function of frequency from 300 kHz to 5 MHz. The arrow indicates the direction of increasing frequency.

The irradiation is performed in a 10-keV ARACOR X-ray source at a dose rate of 31.5 krad(SiO_2)/min at room temperature. During irradiation, the gate is biased with all the other terminals grounded. We have found that there is a relatively high density of pre-existing traps in the gate oxide of these devices, which cause charge trapping due to electrical stress. To account for this, the electrical stress-induced degradation without irradiation is also measured at biases and times comparable to those used in the irradiation experiments. Current-voltage (I-V) characteristics are measured using an Agilent 4156 parameter analyzer. Devices with three different channel lengths are studied. At least three devices of each channel length are tested for each bias condition with and without exposure to X-ray irradiation. After irradiation, the devices are annealed with all terminals grounded at room temperature and remeasured after different annealing times.

RESULTS AND DISCUSSION

Tests were performed with gate voltages (V_{GS}) of +1.0 V, -1.0 V and all the other terminals grounded. All the tested devices have initial threshold voltage of approximately 0.1 V. Fig. 2 (a) shows the I_D (drain current) vs. V_{GS} and G_M (transconductance) vs. V_{GS} at V_{DS}=50 mV as a function of dose up to 2 Mrad(SiO_2) at V_{GS} = +1.0 V during irradiation. The threshold voltage shifts positively, indicating net electron trapping during positive biased irradiation. The leakage current changes negligibly during irradiation, while the ON current (at V_{GS} -V_{TH} = 0.5 V) decreases 26% after 2 Mrad(SiO_2) exposure. Similarly, the peak-G_M degrades 30% at the maximum dose level. However, after a total dose of 2 Mrad(SiO_2), the devices still have an excellent ON/OFF ratio, above 10^5, suggesting excellent gate control. Fig. 2 (b) shows the subthreshold swing (SS), extracted from Fig. 2 (a), as a function of total dose and anneal time. The average SS increases approximately 40 mV/decade, which would correspond to the generation of 2.5×10^{13} $cm^{-2}eV^{-1}$ interface traps, if interface traps were solely responsible for the increase of SS. That the peak-G_M also degrades with dose suggests that there are interface or near interface oxide (border) traps generated during irradiation [9], [10]. The recovery in SS and peak-G_M during annealing is likely related with electron detrapping from the border traps, as we will discuss in the full paper.

To separate the pure TID response from the total response, the bias-induced degradation is measured at biases and times comparable to those used during irradiation. Fig. 2(c) shows the threshold voltage as a function of equivalent dose for (1) TID irradiation, (2) bias only, and (3) the TID response, adjusted for charge trapping due to the simultaneous bias-stress. For the bias-only condition, there is a positive threshold-voltage shift of about 200 mV, indicating an areal density of 7.5×10^{12} cm^{-2} of trapped electrons when projected to the interface. Subtracting the bias-induced threshold-voltage shift from the biased irradiation-induced threshold-voltage shift, there is a negative threshold voltage shift of about 100 mV, which corresponds to an areal density of 3.6×10^{12} cm^{-2} trapped holes when projected to the interface. The net electron trapping suggests that TID-induced hole trapping is less than the bias-induced electron trapping and they partially compensate each other in the threshold voltage shift, as is also observed in HfO_2 gate stack Si nMOSFETs [11]. These results suggest that the TID response of the devices biased at V_{GS} = +1.0 V is dominated by positive bias instability, which is an important issue for InGaAs MOSFETs [6].

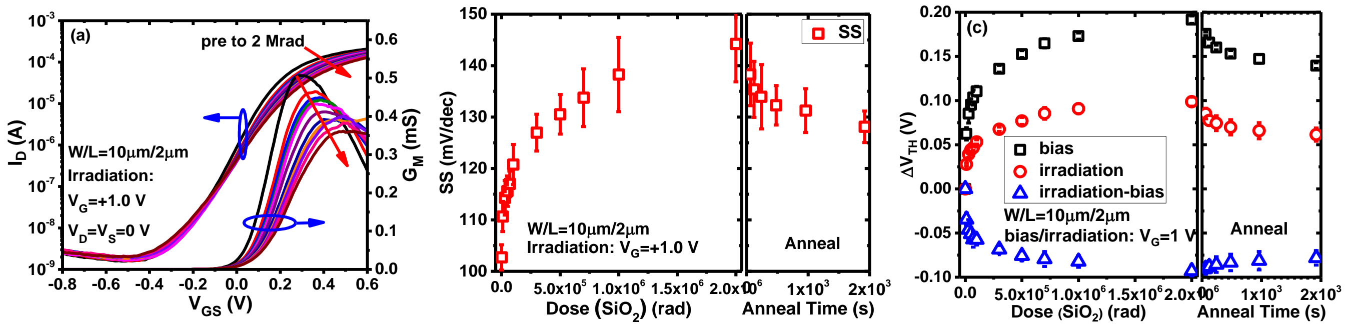

Fig. 2. (a) I_D versus V_{GS} (left) and G_M versus V_{GS} (right) at different irradiation doses for device with L_G = 2 μm. The red arrow indicates the direction of increasing dose. The device is biased at V_{GS} = +1.0 V during irradiation. (b) Subthreshold swing as a function of irradiation dose and annealing time. (c) Threshold voltage as a function of equivalent irradiation dose and annealing time for irradiation, bias only, and the radiation response adjusted to account for the bias stressing effects. The error bars represent standard deviations among different devices tested. Measurements are made with V_{DS} = 50 mV.

Fig. 3 (a) shows I_D vs. V_{GS} and G_M vs. V_{GS} curves as a function of dose up to 2 Mrad(SiO_2) at V_{GS} = -1.0 V during irradiation. In contrast to positive-biased irradiation, the threshold voltage shifts negatively, indicating net hole trapping. The degradation of ON current (at V_{GS} -V_{TH} = 0.5 V) is approximately 7% after 2 Mrad(SiO_2) exposure, significantly smaller than positive biased irradiation. And the SS and peak-G_M also degrade with total dose. As shown in Fig. 3(b), the SS increases by 20 mV/decade, which would correspond to 1.2×10^{13} $cm^{-2}eV^{-1}$ interface traps if the SS increase were caused by interface-trap generation only. As in Fig. 2, it is likely that a combination of interface and border traps lead to the increase in the SS. The corresponding reduction in peak-G_M is 10%. The amount of degradation of both SS and peak-G_M is less than half that measured during positive-biased irradiation. Similar to the positive-bias condition, the bias-induced

threshold voltage shift is measured and subtracted from the TID results to get the bias-stress-adjusted irradiation response. Fig. 3 (c) shows the threshold voltage shift for (1) TID irradiation, (2) bias only, and (3) bias-stress-adjusted TID. There is negligible threshold-voltage shift produced by bias alone. As a result, there is a negative threshold-voltage shift of approximately 60 mV produced by TID alone, which corresponds to 2.2×10^{12} cm^{-2} net hole trapping in the HfO_2.

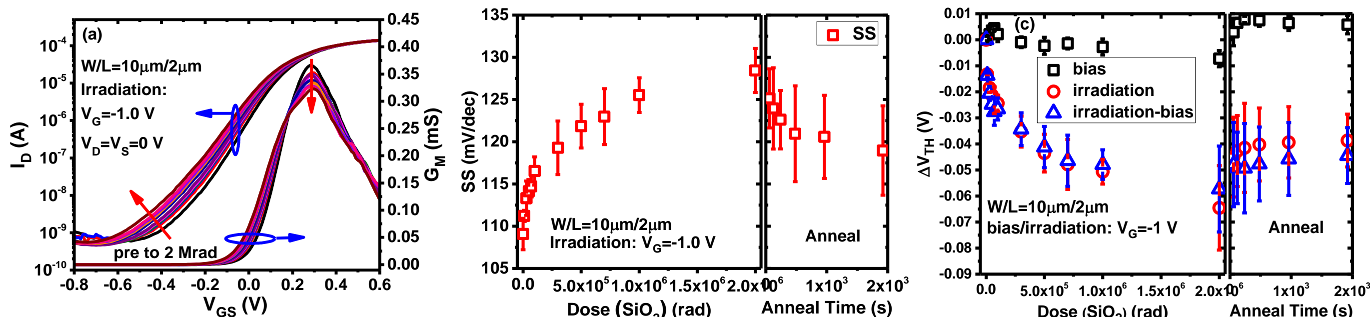

Fig. 3. (a) I_D versus V_{GS} (left) and G_M versus V_{GS} (right) at different irradiation doses for devices with L_G = 2 µm. The red arrow indicates the direction of increasing dose. The device is biased at V_{GS} = -1.0 V during irradiation. (b) Subthreshold swing as a function of dose and annealing time. (c) Threshold voltage as a function of irradiation dose and annealing time for irradiation, bias only, and bias-stress-adjusted irradiation conditions. The error bars represent the standard deviations among different devices tested. Measurements are made with V_{DS} = 50 mV.

Comparison of the radiation responses between V_{GS} = +1.0 V and V_{GS} = -1.0 V suggests that the threshold voltage shift due to irradiation alone is greater for positive gate bias during irradiation than negative gate bias, similar to what is observed in Si MOSFETs with HfO_2 gate oxides [12], and contrary to what is observed in InGaAs gate-all-around MOSFETs [4]. This is due to the differences in gate electric fields at different gate biases, which influence the charge trapping efficiency, as will be discussed in the full paper. The hole trapping during irradiation is less than the bias-induced electron trapping, leading to a net positive threshold voltage shift at V_{GS} = +1.0 V. The radiation-induced hole trapping has the same polarity as the bias-induced hole trapping for irradiation at V_{GS} = -1.0 V, resulting in a net negative threshold-voltage shift.

Fig. 4 (a) shows the transfer characteristics before irradiation and after 2 Mrad(SiO_2) exposure for three devices with three different gate lengths. The device is stressed with V_{GS} = +1.0 V during irradiation. Devices with different gate lengths have similar irradiation response, namely positive threshold-voltage shifts, with negligible leakage-current increase and ON-current degradation. After 2 Mrad(SiO_2) exposure, the devices still have excellent ON/OFF ratios, even for the devices with L_G = 80 nm. The bias-stress-adjusted TID responses are shown in Figs. 4 (b) and (c), respectively, as a function of dose and anneal time for different gate lengths biased at V_{GS} = +1.0 V and V_{GS} = -1.0 V. The results indicate that, the longer the channel, the more pronounced the threshold-voltage shift, for both positive and negative biased irradiations. This suggests there is more hole trapping in the longer device than the shorter devices. This most likely results from electric field variations in the gate dielectric with channel length, which can strongly influence the amount of hole trapping, as we will discuss in the full paper.

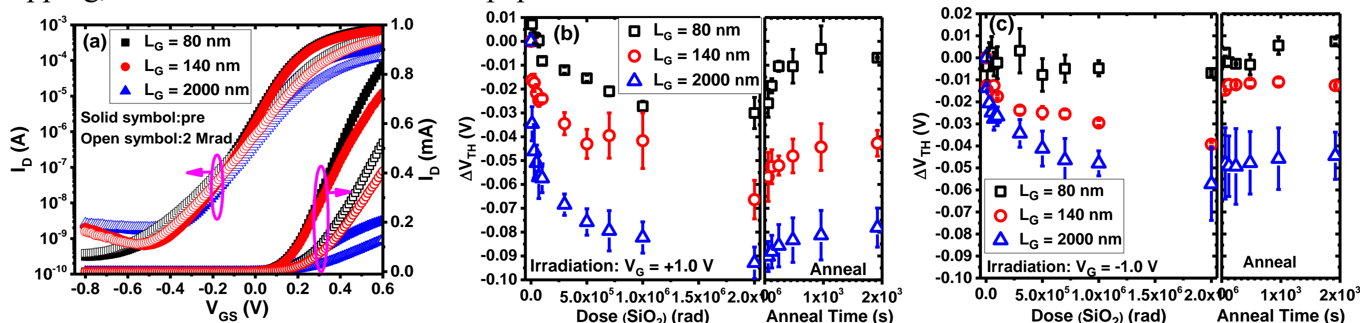

Fig. 4. (a) I_D versus V_{GS} on a linear scale (right) and on a log scale (left) before and after 2 Mrad(SiO_2) irradiation for devices with different gate lengths. During irradiation, V_{GS} = +1.0 V. The bias-stress-adjusted TID-induced threshold voltage shift is shown as a function of dose and anneal time for different gate lengths for bias at (b) V_{GS} = +1.0 V, and (c) V_{GS} = -1.0 V. The error bars represent standard deviations among different devices tested. Measurements are made with V_{DS} = 50 mV.

CONCLUSIONS

The gate bias and geometry dependence of TID effects on InGaAs quantum-well MOSFETs with thin HfO_2 gate oxide have been investigated. Positive gate bias during irradiation leads to bias-stress-induced electron trapping that partially offsets hole trapping, leading to a net positive threshold-voltage shift under the conditions of this study. Negative gate bias during irradiation results in additive hole trapping from both irradiation and bias-stress. The shift produced by the irradiation alone is negative and larger with positive gate bias than that observed under negative gate bias. In addition, the bias-stress-adjusted radiation-induced hole trapping increases with the channel length for both positive and negative biased irradiation. These results provide important, early insight into the mechanisms and magnitude of the combined bias-stress and TID responses of InGaAs quantum-well MOSFETs with thin HfO_2 gate oxide.

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